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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/027,939	12/20/2001	Xia Dai	P9738	2581

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EXAMINER	
STOYNOV, STEFAN	
ART UNIT	**PAPER NUMBER**
2116	

DATE MAILED: 10/13/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/027,939	DAI ET AL.	
	Examiner	Art Unit	
	Stefan Stoynov	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 December 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-7,12-14,17,19 and 22-25* is/are rejected.

7)☐ Claim(s) *2,8-11,15,16,18,20,and 21* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Specification

The following guidelines illustrate the preferred layout for the specification of a utility application. These guidelines are suggested for the applicant's use.

Arrangement of the Specification

As provided in 37 CFR 1.77(b), the specification of a utility application should include the following sections in order. Each of the lettered items should appear in upper case, without underlining or bold type, as a section heading. If no text follows the section heading, the phrase "Not Applicable" should follow the section heading:

(a) TITLE OF THE INVENTION.
(b) CROSS-REFERENCE TO RELATED APPLICATIONS.
(c) STATEMENT REGARDING FEDERALLY SPONSORED RESEARCH OR DEVELOPMENT.
(d) INCORPORATION-BY-REFERENCE OF MATERIAL SUBMITTED ON A COMPACT DISC (See 37 CFR 1.52(e)(5) and MPEP 608.05. Computer program listings (37 CFR 1.96(c)), "Sequence Listings" (37 CFR 1.821(c)), and tables having more than 50 pages of text are permitted to be submitted on compact discs.) or
REFERENCE TO A "MICROFICHE APPENDIX" (See MPEP § 608.05(a). "Microfiche Appendices" were accepted by the Office until March 1, 2001.)
(e) BACKGROUND OF THE INVENTION.
(1) Field of the Invention.
(2) Description of Related Art including information disclosed under 37 CFR 1.97 and 1.98.
(f) BRIEF SUMMARY OF THE INVENTION.
(g) BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWING(S).
(h) DETAILED DESCRIPTION OF THE INVENTION.
(i) CLAIM OR CLAIMS (commencing on a separate sheet).
(j) ABSTRACT OF THE DISCLOSURE (commencing on a separate sheet).
(k) SEQUENCE LISTING (See MPEP § 2424 and 37 CFR 1.821-1.825. A "Sequence Listing" is required on paper if the application discloses a nucleotide or amino acid sequence as defined in 37 CFR 1.821(a) and if the required "Sequence Listing" is not submitted as an electronic document on compact disc).

The disclosure is objected to because of the following informalities:

Brief Summary of Invention missing.

Appropriate correction is required.

Claim Rejections - 35 USC § 101

35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

Claims 24 and 25 are rejected under 35 U.S.C. 101 because the claimed invention lacks patentable utility. In claims 24 and 25 the use of the terminology "if" renders the execution of machine-readable instructions to be optional.

Claim Rejections - 35 USC § 102

> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 3-7, 12-14, 17, and 22 are rejected under 35 U.S.C. 102(b) as being anticipated by Tatsu.

Re claim 1, Tatsu discloses a processor (11) comprising a voltage supply input port (not shown) to receive a first voltage level (normal mode) and a cache (13) to flush or maintain, depending on a power status signal (paragraph 0017, lines 2-4 and paragraph 0019; in Tatsu the flushing or maintaining of the cache contents depends on the residual electric energy of a dc-battery which is an indication of the voltage level and thus is a power status signal), its contents upon entering a low power state (power-saving mode).

Tatsu does not specifically address the voltage level in the low power state. However, the voltage level must necessarily be lower during the low power state and

thus Tatsu inherently discloses a second voltage level wherein the second voltage level is lower than the first voltage level.

Re claim 3, Tatsu discloses the processor (11) of claim 1, further comprising a power status signal port (not shown) from an external source (dc-battery); and a core (paragraph 0023, lines 3 and 4) to receive the power status signal and to flush or maintain the contents of the cache (13) depending on the power status signal (paragraph 0017, lines 2-4 and paragraph 0019).

Re claim 4, Tatsu discloses the processor (11) of claim 1, further comprising a core (paragraph 0023, lines 3 and 4) to generate the power status signal and to flush or maintain the contents of the cache (13) depending on the power status (paragraph 0017, lines 2-4 and paragraph 0019).

Re claim 5, Tatsu discloses the processor (11) of claim 1, further comprising a core to execute instructions; and a phase locked loop to provide clock signal to the core, the cock signal to be off (paragraph 0025) during the low power state (power-saving mode).

Re claim 6, Tatsu discloses the processor (11) of claim 1, wherein the cache is an L1 cache, an L2 cache (paragraph 0019), or both.

Re claim 12, Tatsu discloses a computer system (Drawing 1) comprising a voltage regulator to supply voltage (not shown) at lower level while in low power state (power-saving mode); a cache (13), to be powered by the voltage from the voltage regulator; and a power manager to send a first or second signal (paragraph 0017, lines 2-4 and paragraph 0019) if power reduction associated with maintaining contents of the

cache upon entering the low power state is a lower or higher priority, respectively, than avoiding an increase in a soft error rate in the cache associated with the low power state.

Re claim 13, Tatsu discloses the computer system (Drawing 1) of claim 12, wherein the cache (13) is to flush or maintain (paragraph 0017, lines 2-4 and paragraph 0019) its contents if the processor (11) receives the first or second signal, respectively, upon entering the low power state (power-saving mode).

Re claim 14, Tatsu discloses the computer system (Drawing 1) of claim 13, further comprising a clock to provide a clock signal to a core of a processor (11) containing the cache (13), the clock signal to the core to be off (paragraph 0033) during the low power state (power-saving mode).

Re claim 17, Tatsu discloses a computer system (Drawing 1) comprising a voltage regulator to supply voltage (not shown); a clock to provide clock signal (paragraph 0023); and a processor (11) to receive the clock signal (paragraph 0026) and the voltage, the processor including a cache (13), the processor to flush or maintain, depending on a power status signal (paragraph 0017, lines 2-4 and paragraph 0019), contents of the cache upon entering a low power state (power-saving mode) in which the clock is off (paragraph 0033) and the voltage is reduced.

Re claim 22, Tatsu discloses a method comprising a processor (11) of a computer system (Drawing 1) to enter a low power state (power-saving mode) in which a voltage supplied to a cache (13) of the processor is reduced and a clock supplied to the processor is off (paragraph 0033); and flushing or maintaining contents of cache

upon entering the low power state depending on a power status signal (paragraph 0017, lines 2-4 and paragraph 0019).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 7, 19, and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tatsu in view of Reneris.

Re claim 7, Tatsu describes a processor (11) of claim 1, wherein the cache (13) is to flush its contents upon entering the low power state (power-saving mode) based on a power status signal.

Tatsu fails to disclose the power status signal indicating suspend mode.

Reneris teaches a processor, wherein the cache is to flush its contents upon entering the low power state if the power status signal indicates that a system in which the processor resides is to be suspended (column 12, lines 65-67). After flushing the cache, the power manager powers down the cache, thus achieving greater power savings (column 3, lines 30-35). It would have been obvious to one of ordinary skill in the art at the time of applicant's invention to use the procedure when suspend power state is called, as suggested by Reneris for the power status signal disclosed by Tatsu.

Re claim 19, Tatsu describes a computer system (Drawing 1) of claim 17, wherein the voltage regulator is to supply the voltage (not shown) to the processor (11) at a reduced voltage level during the low power state (power-saving mode), and the cache (13) is to flush its contents upon entering the low power state based on a power status signal.

Tatsu fails to disclose the power status signal indicating suspend mode.

Reneris teaches a computer system, wherein the cache is to flush its contents upon entering the low power state if the power status signal indicates that the computer system is to be suspended (column 12, lines 65-67). After flushing the cache, the power manager powers down the cache, thus achieving greater power savings (column 3, lines 30-35). It would have been obvious to one of ordinary skill in the art at the time of applicant's invention to use the procedure when suspend power state is called, as suggested by Reneris for the power status signal disclosed by Tatsu.

Re claim 23, Tatsu describes the method of claim 22, further comprising flushing the contents of the cache (13) upon entering the low power state (power-saving mode), based on a power status signal.

Tatsu fails to disclose the power status signal indicating suspend mode.

Reneris teaches a method, wherein flushing of the cache upon entering the low power state if the computer system is to be suspended (column 12, lines 65-67). After flushing the cache, the power manager powers down the cache, thus achieving greater power savings (column 3, lines 30-35). It would have been obvious to one of ordinary skill in the art at the time of applicant's invention to use the procedure when suspend power state is called, as suggested by Reneris for the power status signal disclosed by Tatsu.

Claim Objections

Claims 2, 8-11, 15, 16, 18, 20, and 21 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Allowable Subject Matter

The following is a statement of reasons for the indication of allowable subject matter:

Re claim 2, the prior art fails to disclose or suggest "the second voltage level is less than twice an average threshold voltage of a majority of transistors of the processor".

Re claims 8 and 9, the prior art fails to disclose or suggest "that power reduction associated with maintaining the contents of the cache upon entering the low power state is a lower priority than avoiding an increase in a soft error rate in the cache associated with reducing the voltage to the second voltage level".

Re claims 10 and 11, the prior art fails to disclose or suggest "that power reduction associated with maintaining the contents of the cache upon entering the low power state is a higher priority than avoiding an increase in a soft error rate in the cache associated with reducing the voltage to the second voltage level".

Re claims 15, 16, and 18, the prior art fails to disclose or suggest "the second voltage level is less than twice an average threshold voltage of a majority of transistors of the cache".

Re claim 20, the prior art fails to disclose or suggest "the cache to maintain its contents upon entering the low power mode if the power status signal indicates that the voltage is being provided by a battery".

Re claim 21, the prior art fails to disclose or suggest " the cache is to flush its contents upon entering the low power state if the power status signal indicates that the voltage is being provided by an electrical power outlet".

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stefan Stoynov whose telephone number is 703-305-4247. The examiner can normally be reached on 8:00AM-4:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Browne can be reached on 703-308-1159. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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SUPERVISORY PATENT EXAMINER
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